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DOCKET NO. 97-C-108 (STMI01-97108) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	Tsiu Chiu Chan, et al.
Serial No.	:	09/160,824
Filed	:	September 25, 1998
For	:	STACKED MULTI-COMPONENT INTEGRATED CIRCUIT MICROPROCESSOR
Group No.	:	2826
Examiner	:	T. L. Dickey

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PATENT & TRADEMARK OFFICE

DOCKET NO. 97TC108 (STMI01-97108) PATENT
Customer No. 30425

11/12/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Group No.	:	2826
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BOX AF
Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

APPELLANTS' BRIEF ON APPEAL

This Brief is submitted in triplicate on behalf of Appellants for the application identified above. A check is enclosed for the $320.00 fee for filing a Brief on Appeal. Please charge any additional necessary fees to Deposit Account No. 50-0208.

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REAL PARTY IN INTEREST

The real party in interest for this appeal is the assignee of the application, STMICRO-ELECTRONICS, INC. (formerly SGS-THOMSON MICROELECTRONICS, INC.).

RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to the present application which are currently pending.

STATUS OF CLAIMS

Claims 1–20 are pending in the present application. Claim 20 was withdrawn from consideration following a restriction requirement. Claims 7 and 9 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification. Claims 1, 3–4, 6, 8, 10–11, 13–14, 16 and 18 were rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,677,567 to *Ma et al.* Claims 2, 5, 15 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al.* Claims 12 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al* in view of U.S. Patent No. 5,869,895 to *Raad.* The rejection of pending claims 1–19 is appealed.

STATUS OF AMENDMENTS

No amendment to the claims was filed following the final Office Action mailed May 3, 2002.

SUMMARY OF THE INVENTION

The present invention relates to forming integrated circuits. In the present invention, one integrated circuit chip 12, having an active face on which electronic components 30 comprising logic for a central processing unit and contact pads 20 are formed, serves as a base on which a second integrated circuit 14 is mounted:

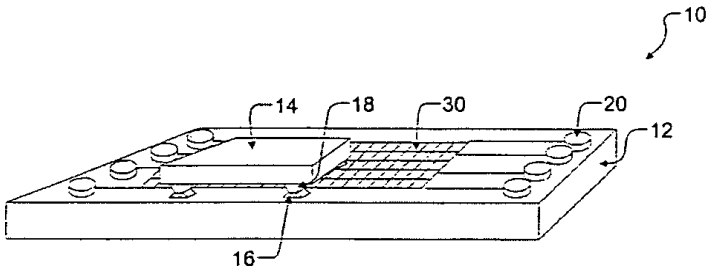

Figure 1

The integrated circuits 12 and 14 are mounted with active areas facing and preferably spaced apart by insulative projections 18 covered by conductive material to form electrical connection between the two integrated circuits:

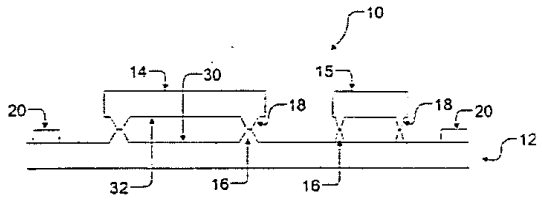

Figure 2

The second integrated circuit is preferably smaller in length and width than the first integrated circuit, to prevent interference with use of wire bonding to connect contact pads 20 to external connections (pins or leads). A third integrated circuit 15 may be mounted on the first integrated circuit 12 adjacent the second integrated circuit 14.

ISSUES ON APPEAL

Claims 7 and 9 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification. Claims 1, 3–4, 6, 8, 10–11, 13–14, 16 and 18 were rejected under 35 U.S.C. § 102(a) as being anticipated by *Ma et al.* Claims 2, 5, 15 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al.* Claims 12 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al* in view of *Raad.* The issues on appeal are:

1. Whether claims 7 and 9 were properly rejected under 35 U.S.C. § 112, first paragraph;
2. Whether 1, 3–4, 6, 8, 10–11, 13–14, 16 and 18 were properly rejected under 35 U.S.C. § 102(a) as being anticipated by *Ma et al*;
3. Whether claims 2, 5, 15 and 17 were properly rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al*; and
4. Whether claims 12 and 19 were properly rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al* in view of *Raad.*

GROUPING OF CLAIMS

Claims 7 and 9 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification. Claims 1, 3–4, 6, 8, 10–11, 13–14, 16 and 18 were rejected under 35 U.S.C. § 102(a) as being anticipated by *Ma et al.* Claims 2, 5, 15 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al.* Claims 12 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al* in view of *Raad.* For purposes of this appeal, the pending claims will be grouped together as follows:

Group A – claims 7 and 9;

Group B – claims 1–19 (all pending rejected claims);

Group C – claim 11;

Group D – claims 10 and 18;

Group E – claim 12;

Group F – claim 14; and

Group G – claim 19.

Groups A–G stand or fall independently. Patentability of the claims within each group is argued separately below.

DISCUSSION OF THE CITED REFERENCES

Ma et al

Ma et al discloses, in an embodiment depicted in Figure 5, two integrated circuit die 502 and 504 mounted on opposite sides of of a lead frame paddle 402 and fingers 404, with conductive bond pads 506 and 516 on the respective die connected to the lead frame paddle 402 and fingers 404 by conductive columns 512 and 520, and the assembly held together by a passivation film 514. In an alternative embodiment depicted in Figure 7, *Ma et al* discloses three integrated circuit die 702, 704 and 706 similarly mounted on opposite sides of a lead frame paddle 710 and fingers 708, with one integrated circuit die 702 on one side and two integrated circuit die 704 and 706 on the other side.

Raad

Raad discloses, in Figure 1, memory devices 103 mounted on an electrical contact frame 109, which in turn is mounted on a microprocessor 101.

ARGUMENT

Group A

Claims 7 and 9 of Group A were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time of the application was filed, had possession of the claimed invention. These claims are properly

grouped together and considered separately from the claims of Groups B–G since they are both subject to a common grounds of rejection that differs from the grounds of rejection addressed in connection with Groups B–G.

Claims 7 and 9 were rejected under the written description requirement of 35 U.S.C. § 112, first paragraph as containing the limitation of "contact pads on the active surface of the first integrated circuit chip for external connection to the central processing unit," which the final Office Action asserts is not supported by the original disclosure.

The test for determining compliance with the written description requirement is whether the disclosure of the application as originally filed reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter, rather than the presence or absence of literal support in the specification for the claim language. MPEP § 2163.02; *In re Kaslow*, 707 F.2d 1366, 1375, 217 U.S.P.Q. 1089, 1096 (Fed. Cir. 1983); *In re Edwards*, 558 F.2d 1349, 1351, 196 U.S.P.Q. 465, 467 (CCPA 1978); *In re Herschler*, 591 F.2d 693, 701, 200 U.S.P.Q. 711, 717 (CCPA 1979). To satisfy the written description requirement, the claimed invention need not be expressed *ipsis verbis* in the original specification. MPEP § 2163.02; *In re Wertheim*, 541 F.2d 257, 262, 190 U.S.P.Q. 90, 96 (C.C.P.A. 1976) ("It is not necessary that the application describe the claim limitations exactly, . . . but only so clearly that persons of ordinary skill in the art will recognize from the disclosure that appellants invented processes including those limitations."); *In re Wright*, 866 F.2d 422, 425, 9 U.S.P.Q.2d 1649, 1651 (Fed.

Cir. 1989) ("[T]he claimed subject matter need not be expressed *in haec verba* in the specification in order for that specification to satisfy the written description requirement."). The fact that the exact words in question may not be in the specification is not important. *In re Wright*, 866 F.2d 422, 425, 9 U.S.P.Q.2d 1649, 1651 (Fed. Cir. 1989).

As noted in Applicants' response to the final Office Action, the specification as filed depicts such pads 20 in Figures 1 and 2, and also contains a description of such pads:

> . . . Finally, disposed on the same surface of the integrated circuit chip 12 as the electrical contacts 16, are pads 20 that serve to connect the integrated circuit microprocessor 10 with a mother or sister-board.
>
> Figure 2 is a cross-sectional side view of an integrated circuit microprocessor 10 made in accordance with the present invention. In order to provide for the electrical connection of the integrated circuit microprocessor 10, the pads 20 are located so as to permit the deposition of solder balls, solder columns or connection by wire bonding for connection with, e.g., a printed circuit board such as a mother or sister board.

Specification, page 13, lines 7–19. In the Advisory Action mailed July 25, 2002, Examiner Thomas L. Dickey asserts:

> [W]ith regard to applicant's argument concerning the 112 rejection of claims 7 and 9, applicant proposes to include 1) contact pads 2) a central processing unit, and 3) connection therebetween in the claimed invention. The passages applicant cites show only a motherboard or sisterboard, not a central processing unit, connected to the contact pads.

Paper No. 9, page 2. However, the rejection in the final Office Action merely stated:

> The limitation "contact pads on the active surface of the first integrated circuit chip for external connection to the central processing unit," which appears in both claims, is not supported by the original disclosure.

Paper No. 7, page 2. This rejection is ambiguous at best, and since the actual claim limitation does not specify connection between the contact pads and the central processing unit, the precise subject matter that Examiner Thomas L. Dickey asserts is not adequately described in the specification is unclear.

Nonetheless, the specification provides adequate written description for this recited claim limitation. Figure 1 depicts an integrated circuit chip 12 having a central processing unit formed by active components 30 on an active face thereof, together with contacts pads 20 and connections between the contact pads 20 and the active components 30 forming the central processing unit:

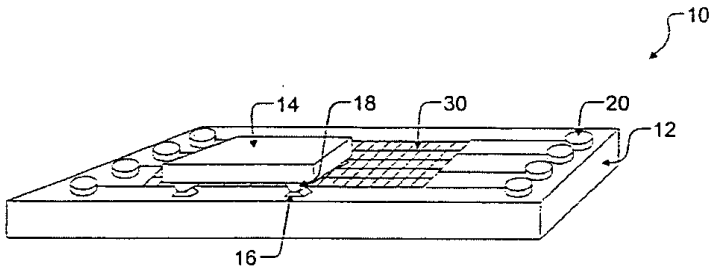

Figure 1

Taken alone, Figure 1 provides adequate written descriptive support for the claim limitation at issue. However, the specification teaches one integrated circuit chip includes a central processing unit within the active face, as well as contact pads connected thereto:

> One embodiment of the present invention is a microprocessor including a first integrated circuit chip, having an active face including a central processing

> unit . . . . The integrated circuit microprocessor 10 has a first integrated circuit chip 12, shown here with the active components 20 and the backside of the silicon not having any active circuit disposed thereon face down. The amount and types of electronic circuits that are disposed as active components 30 integral with the integrated circuit chip 12 will depend on the specific logic processor required. Types of integrated circuits that may be used include the logic necessary to provide a central processing unit, such as, a digital signal processor or an ASIC processor. . . . Finally, disposed on the same surface of the integrated circuit chip 12 as the electrical contacts 16, are pads 20 that serve to connect the integrated circuit microprocessor 10 with a mother or sister-board.

Specification, page 5, lines 22–24; page 11, line 21 through page 12, line 7; and page 13, lines 7–10. Those of ordinary skill in the relevant art are well versed with the use of contact pads to provide external connection to integrated circuitry such as the circuit forming the logic for a central processing unit.

Group B

Claims 1, 3–4, 6, 8, 10–11, 13–14, 16 and 18 of Group B were rejected under 35 U.S.C. § 102(a) as being anticipated by *Ma et al.* Claims 2, 5, 15 and 17 of Group B were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al.* Claims 12 and 19 of Group B were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al* in view of *Raad.* These claims are properly grouped together and considered separately from the claims of Groups A and C–G since (a) they are subject to a different grounds of rejection that than addressed in connection with Group A, (b) they are subject to a common grounds of rejection and contain common limitations distinguishing the claims over the cited references, and (c) a

decision with respect to the claims of Group B may obviate the need for consideration of Groups C–G.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

As noted in response to both Office Actions, independent claims 1 and 13 each recite that the second (integrated circuit) chip is mounted on the active face of the first (integrated circuit) chip. Such a feature is not shown or suggested by the cited reference. The cited portion of *Ma et al* discloses integrated circuits 702 and 704/706 mounted on opposite sides of a single lead frame die paddle 708. *Ma et al* does not teach or suggest mounting one integrated circuit on the active surface of another integrated circuit.

The final Office Action fixed on the use of the term "directly" in the response to the previous Office Action and the absence of that term from the claims. In response to the final Office Action, Applicants noted that the claim term "on" is normally interpreted as requiring direct contact, as opposed to reciting that the chip is mounted "over" the active face, where the

claim term "over" is normally interpreted as permitting intervening layers. In the Advisory Action, however, Examiner Thomas L. Dickey asserts:

> [A]pplicant insists on too narrow a reading of his claim term "on." "On" means "on top of" or "disposed over." Such a reading is supported by applicant's specification as well as being the ordinary meaning of this term. Applicant's reading of this term to mean, "directly connected," is contradicted at various places in applicants specification, where it is disclosed that applicant's invention contemplates spacing the integrated circuit chips apart, as needed, to accomplish applicant's goal. For example see claim 7, where the chips are spaced apart by at least the sum of two projection heights.

Paper No. 9, page 2. The term "on" means <u>on</u> ("so as to be or remain supported by"), NOT "over" as asserted by Examiner Thomas L. Dickey. "On" is ordinarily employed to indicate direct <u>contact</u> (not "direct connection") as opposed to separation by intervening materials. With regard to the integrated circuit chips being spaced apart, portions of facing surfaces of the two integrated circuit chips 12 and 14 are spaced apart in the exemplary embodiment, but the projections 16 and 18 directly contact, so that integrated circuit 14 is <u>on</u> integrated circuit 12:

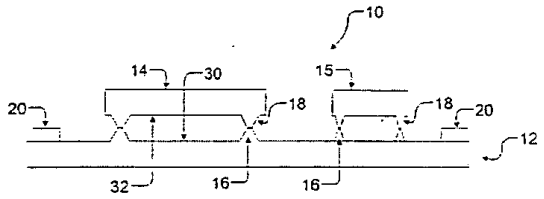

Figure 2

The ordinary meaning of the term "on" is plain, and the claim limitation of the second chip being "on" the active surface of another integrated circuit is not shown or suggested by *Ma et*

al, since *Ma et al* only discloses integrated circuits which are "on" opposite faces of a lead frame.

Group C

Claim 11 of Group C was rejected under 35 U.S.C. § 102(a) as being anticipated by *Ma et al*. This claim is properly considered separately from the claims of Groups A–B and D–G since (a) it is subject to a different grounds of rejection that than addressed in connection with Group A, (b) it contains a limitation distinguishing the claim over the cited reference(s) not found in the claims of Groups B and D–G: direct connection of the metal regions on the active faces of the first and second integrated circuit chips by a bonding layer.

The lead frame of *Ma et al* is not a bonding layer, providing no "bonding", which is provided in *Ma et al* by passivation film 514. In addition, contact pads 506 and 516 are connected by conductive material 512 and 520 to lead frame paddle 402 and fingers 404, whcih does not satisfy the claim limitation of providing direct connection of metal regions on the active faces of the two integrated circuits. Such a feature is not shown or suggested by the cited reference.

Group D

Claims 10 and 18 of Group D were rejected under 35 U.S.C. § 102(a) as being anticipated by *Ma et al*. These claims are properly grouped together and considered separately from the claims of Groups A–C and D–G since (a) they are subject to a different grounds of

rejection that than addressed in connection with Group A, (b) they contain common limitations distinguishing the claims over the cited reference(s) not found in the claims of Groups B–C and D–G: a third integrated circuit is also mounted on an active face of the first integrated circuit, adjacent to the second integrated circuit.

Such a feature is not shown or suggested by *Ma et al*. *Ma et al* depicts, in Figure 7, two integrated circuits 704 and 706 mounted on one side of a lead frame 708 and a third integrated circuit 702 mounted on the opposite side of the lead frame 708. While integrated circuits 704 and 706 are adjacent, they are not "on" integrated circuit 702.

Group E

Claim 12 of Group E was rejected under 35 U.S.C. § 102(a) as being anticipated by *Ma et al* in view of *Raad*. This claim is properly considered separately from the claims of Groups A–D and F–G since (a) it is subject to a different grounds of rejection that than addressed in connection with Group A, (b) it contains a limitation distinguishing the claim over the cited reference(s) not found in the claims of Groups B–D and F–G: that the length and width of the second integrated circuit chip are less than a respective length and width of the first integrated circuit chip.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie*

basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to

make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

No motivation exists for selectively incorporating a feature from *Raad* into the structure of *Ma et al* as proposed, nor do the references provide any reasonable expectation of success in making the proposed combination.

Group F

Claim 14 of Group F was rejected under 35 U.S.C. § 102(a) as being anticipated by *Ma et al*. This claim is properly considered separately from the claims of Groups A–E and G since (a) it is subject to a different grounds of rejection that than addressed in connection with Group A, (b) it contains a limitation distinguishing the claim over the cited reference(s) not found in the claims of Groups B–E and G: insulating regions projecting from the active faces of the first and second chips and covered by conductive layers.

Such a feature is not shown or suggested by the cited references. Examiner Thomas L. Dickey did not address this claim feature in either the final Office Action or the Advisory Action.

Group G

Claim 19 of Group G was rejected under 35 U.S.C. § 102(a) as being anticipated by *Ma et al* in view of *Raad*. This claim is properly considered separately from the claims of Groups A–F since (a) it is subject to a different grounds of rejection that than addressed in connection

with Group A, (b) it contains a limitation distinguishing the claim over the cited reference(s) not found in the claims of Groups B–F: that the width of the second integrated circuit chip is less than a respective width of the first integrated circuit chip.

No motivation exists for selectively incorporating a feature from *Raad* into the structure of *Ma et al* as proposed, nor do the references provide any reasonable expectation of success in making the proposed combination.

CONCLUSION

The specification provides written description of all claim limitations. Therefore, the rejection under 35 U.S.C. § 112, first paragraph is improper. None of the cited references, taken alone or in combination, show or suggest all features of the invention claimed in Groups A–B. Therefore, the rejection under 35 U.S.C. § 103 is improper. Applicant respectfully requests that the Board of Appeals reverse the decision of the Examiner below rejecting all pending claims in this application.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: 11-12-02

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APPENDIX TO APPELLANT'S BRIEF ON APPEAL
PENDING CLAIMS ON APPEAL

1. (unchanged) A microprocessor comprising:

a first integrated circuit chip having an active face including a central processing unit; and

a second integrated circuit chip mounted on, and electrically connected to, the active face of the first integrated circuit, wherein the second integrated circuit chip provides added functionality to the central processing unit of the first integrated circuit.

2. (amended) The microprocessor of claim 1, wherein the central processing unit comprises one of a digital signal processor and a field programmable gate array.

3. (amended) The microprocessor of claim 1, wherein an active face of the second integrated circuit chip faces the active face of the first integrated circuit chip.

4. (amended) The microprocessor of claim 1, wherein the second integrated circuit chip comprises one of a memory and an analog-to-digital converter.

5. (amended) The microprocessor of claim 4, wherein the second integrated circuit comprises one of a cache memory, a dynamic random access memory (DRAM), a static random access memory (SRAM), and a flash memory.

6. (amended) The microprocessor of claim 1, wherein at least one metal region projecting from the active face of the first integrated circuit chip overlies at least one metal region projecting from a surface of the second integrated circuit chip.

7. (amended) The microprocessor of claim 6, wherein the second integrated circuit chip is spaced apart from the first integrated chip by a distance of at least a projection height of the at least one metal region projecting from the active face of the first integrated circuit chip plus a projection height of the at least one metal region projecting from the surface of the second integrated circuit chip, wherein the distance is sufficient to permit electrical connection to contact pads on the active surface of the first integrated circuit chip for external connection to the central processing unit.

8. (amended) The microprocessor of claim 6, further comprising:

a bonding layer between and electrically connecting the at least one metal region projecting from the active face of the first integrated circuit chip and the at least one metal region projecting from a surface of the second integrated circuit chip, wherein the bonding layer provides mechanical bonding of the first and second integrated circuit chips.

9. (amended) The microprocessor of claim 1, further comprising:

at least two groups of contact pads on the active surface of the first integrated circuit chip for external connection to the central processing unit, wherein the second integrated circuit chip has a width less than a distance between the two groups of contact pads.

10. (amended) The microprocessor of claim 1, further comprising:

a third integrated circuit chip mounted on, and electrically connected to, the active face of the first integrated circuit adjacent the second integrated circuit chip, wherein the third integrated circuit chip adds further functionality to the central processing unit of the first integrated circuit.

11. (amended) The microprocessor of claim 1, wherein the electrical connection between the first integrated circuit chip and the second integrated circuit chip is by direct connection of metal regions on the active faces of the first and second integrated circuit chips by a bonding layer.

12. (amended) The microprocessor of claim 1, wherein a length and width of the second integrated circuit chip are less than a respective length and width of the first integrated circuit chip.

13. (amended) A microprocessor comprising:

a first chip having an active face including a central processing unit; and

a second chip having an active face, the second chip mounted on, and electrically connected to, the active face of the first chip, wherein the second chip adds functionality to the central processing unit of the first chip and wherein the electrical connection is by a bonding layer between metal regions on the active faces of the first and second chips.

14. (amended) The microprocessor of claim 13, wherein the metal regions further comprise one of:

conductive regions projecting from the active faces of the first and second chips; and

conductive layers over insulating regions projecting from the active faces of the first and second chips,

wherein the active regions of the first and second chips are spaced apart by the metal regions.

15. (amended) The microprocessor of claim 13, wherein the central processing unit comprises one of a digital signal processor and a field programmable gate array.

16. (amended) The microprocessor of claim 13, wherein the second chip comprises one of a memory and an analog-to-digital converter.

17. (amended) The microprocessor of claim 13, wherein at least one of the metal regions on the active surface of the first chip is disposed over a portion of an integrated circuit forming the central processing unit.

18. (amended) The microprocessor of claim 13, further comprising:

a third chip mounted on, and electrically connected to, the active face of the first chip adjacent the second chip wherein the third chip adds further functionality to the central processing unit of the first chip.

19. (amended) The microprocessor of claim 13, wherein a width of the second integrated circuit chip is less than a width of the first integrated circuit chip.